

Appl. No. 10/731,078  
Amdt. dated September 7, 2004  
Reply to Office action of June 4, 2004

**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application:

Please cancel claims 1-3 and 21-25 as shown in the listing of claims below:

1-7. (canceled)

8. (previously presented) A method for refreshing a dynamic register, the dynamic register comprising a first transmission gate and a second transmission gate operating in accordance with complementary clock signals, a first inverter disposed between the first and second transmission gates, a second inverter disposed at the output of the second transmission gate, the first inverter having a first input terminal and a first output terminal, the second inverter having a second input terminal and a second output terminal, the method comprising the operations of:

- (a) coupling a feedback path from the first output terminal to the first input terminal to create a first static loop;
- (b) coupling a feedback path from the second output terminal to the second input terminal to create a second static loop;
- (c) providing a control signal separate from the complementary clock signal to the first and second static loops; and
- (d) activating the first and second static loops via the control signal to refresh the dynamic register.

9. (previously presented) The method of claim 8 further comprising:  
setting the control signal equal to approximately zero to deactivate the first and second static loops so that the dynamic register operates in a dynamic mode.

10-13. (canceled)

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comprising a first transmission gate and a second transmission gate operating in accordance with complementary clock signals, a first inverter disposed between the first and second transmission gates, a second inverter disposed at the output of the second transmission gate, the first inverter having a first input terminal and a first output terminal, the second inverter having a second input terminal and a second output terminal, the system comprising:

- (a) a first static loop coupled to the first inverter as a feedback path from the first output terminal to the first input terminal, the first static loop receiving a control signal, the first static loop being activated or deactivated by the control signal, the first static loop refreshing the first inverter when activated; and
- (b) a second static loop coupled to the second inverter as a feedback path from the second output terminal to the second input terminal, the second static loop receiving a control signal, the second static loop being activated or deactivated by the control signal, the second static loop refreshing the second inverter when activated.

15. (original) The system of claim 14 wherein the first and second static loops are deactivated when the control signal is approximately equal to zero.

16-25. (canceled)

26. (previously presented) A data system comprising:

a dynamic circuit element having an input terminal and an output terminal, and that operates in accordance with clocking signals; and

a static loop that forms a feedback path from the output terminal to the input terminal and refreshes the dynamic circuit element in accordance with a control signal.

27. (previously presented) The data system of claim 26 wherein the dynamic circuit element comprises an inverter.

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28. (previously presented) The data system of claim 26 wherein the control signal activates or deactivates the static loop.

29. (previously presented) The data system of claim 28 wherein the static loop refreshes the dynamic circuit when the static loop is activated.